IN THE CLAIMS

1. (Previously Presented) A p-channel depletion mode floating gate transistor, comprising:

a first source/drain region and a second source/drain region separated by a depletion mode p-type channel region in an n-type substrate;

a floating gate opposing the p-type channel region and separated therefrom by a gate oxide;

a control gate opposing the floating gate; and

wherein the control gate is separated from the floating gate by an asymmetrical low tunnel barrier intergate insulator selected to provide a desired first barrier height with respect to the floating gate and a desired second barrier height with respect to the control gate, the first barrier height being different than the second barrier height to promote easier erase operations and longer retention.

2. (Previously Presented) The p-channel depletion mode floating gate transistor of claim 1, wherein the asymmetrical low tunnel barrier intergate insulator includes aluminum oxide (Al_2O_3), wherein the aluminum oxide has a number of small compositional ranges such that compositional gradients are formed to produce different barrier heights at an interface with the floating gate and control gate.

3. (Original) The p-channel depletion mode floating gate transistor of claim 1, wherein the asymmetrical low tunnel barrier intergate insulator includes an asymmetrical transition metal oxide.

4. (Original) The p-channel depletion mode floating gate transistor of claim 3, wherein the asymmetrical transition metal oxide is selected from the group consisting of Ta_2O_5, TiO_2, ZrO_2, and Nb_2O_5.

5. (Original) The p-channel depletion mode floating gate transistor of claim 1, wherein the asymmetrical low tunnel barrier intergate insulator includes an asymmetrical Perovskite oxide tunnel barrier.

6. (Original) The p-channel depletion mode floating gate transistor of claim 5, wherein the asymmetrical Perovskite oxide tunnel barrier is selected from the group consisting of $SrBi_2Ta_2O_3$, $SrTiO_3$, $PbTiO_3$, and $PbZrO_3$.

7. (Original) The p-channel depletion mode floating gate transistor of claim 1, wherein the floating gate includes a polysilicon floating gate having a metal layer formed thereon in contact with the asymmetrical low tunnel barrier intergate insulator.

8. (Previously Presented) The p-channel depletion mode floating gate transistor of claim 7, wherein the control gate includes a polysilicon control gate having a metal layer formed thereon in contact with the asymmetric low tunnel barrier intergate insulator, wherein the metal layer includes a metal layer that has a different work function than the metal layer formed on the floating gate.

9. (Previously Presented) A vertical, p-channel depletion mode non volatile memory cell, comprising:

a first source/drain region formed on a substrate;

a body region including a p-type depletion mode channel region formed on the first source/drain region;

a second source/drain region formed on the body region;

a floating gate opposing the channel region and separated therefrom by a gate oxide;

a control gate opposing the floating gate; and

wherein the control gate is separated from the floating gate by an asymmetrical low tunnel barrier intergate insulator having a number of small compositional ranges such that compositional gradients are formed to produce a first barrier height with the floating gate and a

different second barrier height with the control gate to promote easier erase operations and longer retention.

10. (Original) The vertical, p-channel depletion mode non volatile memory cell of claim 9, wherein the asymmetrical low tunnel barrier intergate insulator includes an insulator selected from the group consisting of Al_2O_3, Ta_2O_5, TiO_2, ZrO_2, Nb_2O_5, $SrBi_2Ta_2O_3$, $SrTiO_3$, $PbTiO_3$, and $PbZrO_3$.

11. (Original) The vertical, p-channel depletion mode non volatile memory cell of claim 9, wherein the floating gate includes a polysilicon floating gate having a metal layer formed thereon in contact with the asymmetrical low tunnel barrier intergate insulator.

12. (Previously Presented) The vertical, p-channel depletion mode non volatile memory cell of claim 11, wherein the control gate includes a polysilicon control gate having a metal layer formed thereon in contact with the asymmetrical low tunnel barrier intergate insulator, wherein the metal layer includes a metal layer that has a different work function than the metal layer formed on the floating gate.

13. (Original) The vertical, p-channel depletion mode non volatile memory cell of claim 9, wherein the floating gate includes a vertical floating gate formed alongside of the body region.

14. (Original) The vertical, p-channel depletion mode non volatile memory cell of claim 13, wherein the control gate includes a vertical control gate formed alongside of the vertical floating gate.

15. (Original) The vertical, p-channel depletion mode non volatile memory cell of claim 9, wherein the floating gate includes a horizontally oriented floating gate formed alongside of the body region.

16. (Original) The vertical, p-channel depletion mode non volatile memory cell of claim 15, wherein the control gate includes a horizontally oriented control gate formed above the horizontally oriented floating gate.

17. (Previously Presented) A non-volatile memory cell, comprising:

a first source/drain region and a second source/drain region separated by a p-type channel region in an n-type substrate;

a polysilicon floating gate opposing the channel region and separated therefrom by a gate oxide;

a first metal layer formed on the polysilicon floating gate;

a metal oxide intergate insulator formed on the metal layer, wherein the metal oxide intergate insulator includes an asymmetrical metal oxide having a number of small compositional ranges such that gradients can be formed in an applied electric field which produce a first barrier height with respect to the floating gate and a different second barrier height with the control gate to promote easier erase operations and longer retention;

a second metal layer formed on the metal oxide intergate insulator, wherein the second metal layer has a different work function from the first metal layer to further promote easier erase operations and longer retention; and

a polysilicon control gate formed on the second metal layer.

18. (Original) The non-volatile memory cell of claim 17, wherein first metal layer includes a parent metal for the asymmetrical metal oxide and the second metal layer includes a metal layer having a work function in the range of 2.7 eV to 5.8 eV.

19. (Original) The non-volatile memory cell of claim 17, wherein the second metal layer is platinum (Pt) and the metal oxide intergate insulator is selected from the group consisting of TiO_2, $SrTiO_3$, $PbTiO_3$, and $PbZrO_3$.

20. (Original) The non-volatile memory cell of claim 17, wherein the second metal layer is aluminum and the metal oxide intergate insulator is selected from the group consisting of Ta_2O_5, ZrO_2, $SrBi_2Ta_2O_3$, $SrTiO_3$, $PbTiO_3$, and $PbZrO_3$.

21. (Original) The non-volatile memory cell of claim 17, wherein the metal oxide intergate insulator is selected from the group consisting of Al_2O_3, Ta_2O_5, TiO_2, ZrO_2, Nb_2O_5, $SrBi_2Ta_2O_3$, $SrTiO_3$, $PbTiO_3$, and $PbZrO_3$.

22. (Original) The non-volatile memory cell of claim 17, wherein the floating gate transistor includes a vertical floating gate transistor.

23. – 83. (Canceled)

84. (New) A p-channel depletion mode floating gate transistor, comprising:

a first source/drain region and a second source/drain region separated by a depletion mode p-type channel region in an n-type substrate;

a floating gate opposing the p-type channel region and separated therefrom by a gate oxide; and

a control gate opposing the floating gate and separated therefrom by an intergate insulator having a metal oxide with compositional gradients to produce a first barrier height with respect to the floating gate and a different second barrier height with the control gate to promote easier erase operations and longer retention.

85. (New) The transistor of claim 84, wherein the floating gate includes a polysilicon floating gate and the control gate includes a polysilicon control gate, further comprising a first metal layer between polysilicon floating gate and the intergate insulator, and a second metal layer between the intergate insulator and the polysilicon control gate, the first and second metal layers having different work functions to further promote easier erase operations and longer retention.

86. (New) The transistor of claim 85, wherein the first metal includes a parent metal for the metal oxide.

87. (New) The transistor of claim 85, wherein the second metal includes platinum.

88. (New) The transistor of claim 85, wherein the second metal includes aluminum.

89. (New) A p-channel depletion mode floating gate transistor, comprising:

a first source/drain region and a second source/drain region separated by a depletion mode p-type channel region in an n-type substrate;

a floating gate opposing the p-type channel region and separated therefrom by a gate oxide; and

a control gate opposing the floating gate and separated therefrom by an intergate insulator having an aluminum oxide with compositional gradients to produce a first barrier height with respect to the floating gate and a different second barrier height with the control gate.

90. (New) A p-channel depletion mode floating gate transistor, comprising:

a first source/drain region and a second source/drain region separated by a depletion mode p-type channel region in an n-type substrate;

a floating gate opposing the p-type channel region and separated therefrom by a gate oxide; and

a control gate opposing the floating gate and separated therefrom by an intergate insulator having a transmission metal oxide with compositional gradients to produce a first barrier height with respect to the floating gate and a different second barrier height with the control gate.

91. (New) The transistor of claim 90, wherein the transition metal oxide includes Ta_2O_5.

92. (New) The transistor of claim 90, wherein the transition metal oxide includes TiO_2.

93. (New) The transistor of claim 90, wherein the transition metal oxide includes ZrO_2.

94. (New) The transistor of claim 90, wherein the transition metal oxide includes Nb_2O_5.

95. (New) A p-channel depletion mode floating gate transistor, comprising:

a first source/drain region and a second source/drain region separated by a depletion mode p-type channel region in an n-type substrate;

a floating gate opposing the p-type channel region and separated therefrom by a gate oxide; and

a control gate opposing the floating gate and separated therefrom by an intergate insulator having a Perovskite oxide with compositional gradients to produce a first barrier height with respect to the floating gate and a different second barrier height with the control gate.

96. (New) The transistor of claim 95, wherein the Perovskite oxide includes $SrBi_2Ta_2O_3$.

97. (New) The transistor of claim 95, wherein the Perovskite oxide includes $SrTiO_3$.

98. (New) The transistor of claim 95, wherein the Perovskite oxide includes $PbTiO_3$.

99. (New) The transistor of claim 95, wherein the Perovskite oxide includes $PbZrO_3$.

Conclusion

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney at (612) 373-6960 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully Submitted,

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Name Amy Moriarty Signature

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Leonard Forbes et al.	Examiner: Tu-Tu V. Ho
Serial No.:	10/028001	Group Art Unit: 2818
Filed:	December 20, 2001	Docket: 1303.035US1
Title:	PROGRAMMABLE ARRAY LOGIC OR MEMORY WITH P-CHANNEL DEVICES AND ASYMMETRICAL TUNNEL BARRIERS	

COMMUNICATION CONCERNING RELATED APPLICATION(S)

MS RCE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Applicants would like to bring to the Examiner's attention the following related application(s) in the above-identified patent application:

Serial/Patent No.	Filing Date	Attorney Docket	Title
09/945395	August 30, 2001	1303.019US1	DRAM CELLS WITH REPRESSED FLOATING GATE MEMORY, LOW TUNNEL BARRIER INTERPOLY INSULATORS
09/943134	August 30, 2001	1303.020US1	PROGRAMMABLE ARRAY LOGIC OR MEMORY DEVICES WITH ASYMMETRICAL TUNNEL BARRIERS
09/945512	August 30, 2001	1303.027US1	IN SERVICE PROGRAMMABLE LOGIC ARRAYS WITH LOW TUNNEL BARRIER INTERPOLY INSULATORS
09/945554	August 30, 2001	1303.028US1	SRAM CELLS WITH REPRESSED FLOATING GATE MEMORY, LOW TUNNEL BARRIER INTERPOLY INSULATORS
10/081818	February 20, 2002	1303.045US1	ATOMIC LAYER DEPOSITION OF METAL OXIDE AND/OR LOW ASYMMETRICAL TUNNEL BARRIER INTERPLOY INSULATORS
10/177096	June 21, 2002	1303.063US1	GRADED COMPOSITION METAL OXIDE TUNNEL BARRIER

			INTERPOLY INSULATORS
Unknown	February 18, 2004	1303.063US2	GRADED COMPOSITION METAL OXIDE TUNNEL BARRIER INTERPOLY INSULATORS

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